REMARKS

The rejections and comments of the Examiner set forth in the Office Action dated April 10, 2001 have been carefully reviewed by the Applicant. Additionally, informalities in the specification have been corrected. No new matter has been added.

Claims 1 and 18 are objected to due to informalities. Claims 1 and 18 have been canceled.

Claims 10-14 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements. Claims 10-14 have been canceled.

Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form. Claim 4 has been canceled.

Claims 1-3, 5-10, 12-14 and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hathaway et al. [U.S. Patent #5,757,657] in view of Shouen [U.S. Patent # 6,086,625]. Claims 1-3, 5-10, 12-14, and 18-21 have been canceled.

New claims 22-26 include the element of "changing the netlist in response to how the cells are placed". This element is supported in the specification at page 8, lines 8-14. Although Hathaway discusses changes to a netlist and changes in the placement of cells, the discussion with respect to cause and effect is limited to changing the placement of cells in response to a change in the netlist. Hathaway does not teach or suggest "changing the netlist in response to how the cells are placed". Shouen also does not

teach or suggest "changing the netlist in response to how the cells are placed". Shouen does not use the term "netlist" at all, but at column 10, line 33 refers to "The logic design information synthesized by the logic synthesis processing unit 3" (synthesis processing unit 3 is shown in FIG. 14). The product of "synthesis" in Shouen is not influenced by how cells are placed, and the logic synthesis processing unit does not use cell placement information as an input. Thus, neither Hathaway nor Shouen, individually or in combination, suggest or changing the netlist in response to how the cells are placed.

New claims 27-31 include the element "changing the size of said placement area". This element is supported in the specification at page 5, lines 8-9. The "placement area" of the present claimed invention is the overall area allotted on a substrate for circuit placement. "design area" of Hathaway and the "predetermined area" of Shouen refer to the overall area allotted on a substrate for circuit placement. Hathaway only teaches or suggests the changing of a "replacement region". The "replacement region" of Hathaway is a subset of the "design area" and is changed in size at the expense of other "replacement regions" without altering the overall "design area", as is shown in FIGs 2-4. Shouen discusses placement and arrangement within a "predetermined area" but does not teach or suggest modifying the "predetermined area". Thus, neither Hathaway nor Shouen, individually or in combination, suggest or teach changing the size of the placement area.

New claims 32-36 include both of the above mentioned elements "changing the size of said placement area" and "changing the netlist in response to how the cells are placed" that are neither taught nor suggested by Hathaway and Shouen.

In summary, Applicants assert Claims 22-36 are now in condition for allowance and earnestly solicit such action by the Examiner.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

1. The second paragraph on page 6 beginning with "The detailed placement process...", has been replaced with the following paragraph:

Often, several iterations of the design, layout, and testing process are required in order to optimize the semiconductor chip's size, cost, heat output, speed, power consumption, and electrical functionalities. However, one problem is attributable to the fact that each of these stages is highly dependent on the results of the other stages. A minor alteration in one stage intended to enhance one characteristic may cause unforeseen problems to occur in other stages. For example, changing a cell in the synthesis stage might drastically alter the current place and route. It is this high degree of interdependence which makes it extremely difficult to predict and account for the consequences associated with any changes. Indeed, the overall design might sometimes be worse in a successive iteration. Furthermore, the iterative process is time-consuming and requires a powerful computer to perform the processing. In addition, the iterative process is labor intensive and requires the dedication of a highly skilled, experienced EDA specialist.

2. The second paragraph on page 12 beginning with "The mapped netlist is input...", has been replaced with the following paragraph:

The mapped netlist is input to a cell separator. Cell separation is then performed in step 306 to assign (x,y) coordinates for each cell in the mapped netlist 305. As described above, the task of cell separation is to calculate the positions of the cells. Since

the quality of the placement determines the minimal achievable area and wiring length of a circuit, placement has a large impact on production yield and circuit performance. Cell separation tools handle the problem of assigning locations to cells (e.g., objects or elements) so as to minimize some overall cost function. In this area, the cost function is related to the wiring distance between cells. Cells must be assigned locations so that they do not overlap each other, they all fit within some overall bounding figure, and the total wiring cost is minimized. The output from cell separation process 306 is a number of cells, each of which has an assigned (x,y) position 307 denoting the approximate centerpoint of the cell. A subroutine call is made back to the synthesis program with the new cell location information 307. Based on this new cell information, the synthesis program then generates a new netlist 309. The (x,y) location of the cells 307 and the new netlist 309 are input to a spacing tool. The spacing step 310 changes the partition walls in order to improve the spacings between the cells. The updated partition wall locations 311 are generated by spacing step 310. Next, the updated partition walls 311 and the new netlist 309 are used to formulate new partitions in step 312. There are a number of different partitioning approaches that can be implemented with the present invention. One such method is disclosed in the article by Ren-Song Tsay, Ernest S. Kuh, and Chi-Ping Hsu, *PROUD: A Fast Sea-Of-Gates Placement Algorithm*, published in the 25th ACM/IEEE Design Automation Conference (1988), paper 22.3. This approach takes advantage of inherent sparsity in the connectivity specification for an integrated circuit design and solves repeatedly sparse linear equations by the SOR (successive over-relaxation) method in a top-down hierarchy. Another approach is disclosed in a paper by Alfred E. Dunlop and Brian W. Kernighan, *A Procedure for Placement of Standard-Cell VLSI Circuits*, published in the IEEE

Transactions on Computer-Aided Design, Vol. CAD-4, No. 1, Jan. 1985. This approach is based on graph partitioning to identify groups of modules that ought to be close to each other, and uses a technique for properly accounting for external connections at each level of partitioning. Other approaches to the partitioning process include min-cut, force-directed, simulated annealing, and spectral approaches.